Impact of Mismatch Cables Impedances on Active Motor Terminal Overvoltage Mitigation Using Parallel Voltage Source Inverters

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***Abstract*—Non-treated transient motor terminal overvoltage due high-speed switching sources and long cable length can be twice the original source voltage amplitude. In some cases, this overvoltage can cause premature motor insulation failure. A topology widely applied in industry is subject of this overvoltage: motors driven by voltage source inverter, connected by long feeding cable. There are several passive methods effective in mitigating overvoltage, but most of them are based in lossy and bulky passive component filters. A different approach is proposed by two low loss active methods for overvoltage mitigation with simple topologies. It consists in using voltage source inverters with specific switching strategy in order to attenuate the main cause of overvoltage: the superposition of traveling reflected pulses at the motor terminals. As promising methods for overvoltage mitigation, some specific studies regarding its particularities must be carried on in order to clear understand all its benefits and possible drawbacks. The present paper discusses the vulnerability of these overvoltage mitigation methods to some internal parameter variation. The impact of cables impedance variation due heating –and impedance mismatch– is highlighted, since it is intrinsic to the system and can degrades overvoltage mitigation.**

***Index Terms*— Electromagnetic transients, Overvoltage protection, AC motor protection, Pulse width modulation inverters, impedance matching.**

I. INTRODUCTION

LARGELY employed in industry, voltage source inverters (VSI) are the most common solution for adjustable-speed motor drives due its performance and flexibility. Fast switching devices based in IGBT and SiC are responsible for reducing VSI switching losses, heatsinks and drive enclosure size and costs [1][2]. However, as switching devices becomes faster, pulse width modulation (PWM) voltage output presents smaller rise and fall time, generating high *dv/dt*. In long cables, high *dv/dt* pulses propagates as traveling waves in transmission lines [1][3]. If pulses propagation delay towards the cable length t_{pd} is higher than half the rise time of the pulses, then a full reflection will happen at the motor terminals [3], generating transient overvoltage that can reach two times the original voltage pulse amplitude. This overvoltage level could cause insulation failure and windings burning, completely shutting down the motor.

In nuclear power plants and offshore plants, many motors and pumps need to be placed far from its voltage feeding source, some of them are related to safety cooling systems. In those cases, mitigate transient overvoltage allows greater reliability and longer shelf life. Also, avoid important plant systems to shut down and put the entire plant in safety risks.

Many passive methods for overvoltage mitigation have been developed in the past years. Most of them aim to convert VSI pulses into a resembling sinus wave - sinusoidal filter [4] - or aim to match cable impedance and terminal motor impedance - cable terminator [5] - or also, aim to reduce pulse rise time - line inductor and *dv/dt* filter [6], [7]. In despite of the effectiveness and reliability of those passive methods, the low flexibility, the use of bulky components and the power losses represent significant drawbacks [7], [8], [9].

This paper aims to investigate active overvoltage mitigation, compare some known methods and present a robustness test of the two parallel inverters method, showing a vulnerability due impedance mismatching of the cables.

The paper is composed as follows: in Section II, pulse propagation through cables and reflection phenomena is discussed, focusing on motor terminal transient overvoltage. In Section III the known active overvoltage mitigation methods are discussed. In Section IV, is proposed the methodology to compare the different mitigation methods and analyze the mismatch impedance impact on overvoltage. In section V, simulation results are presented and discussed. In section VI the conclusions are given.

II. PULSE REFLECTION AND OVERVOLTAGE

During the pulse reflection at the motor terminals, the traveling pulse will be partially transmitted to the motor and partially reflected backwards to the cable, in the opposite direction of the original pulse, as show in Fig. 1. The transient overvoltage amplitude on motor terminals V_m depends on the reflection coefficient Γ_m - a relation between cable and motor terminal impedances - described by:

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{1}$$

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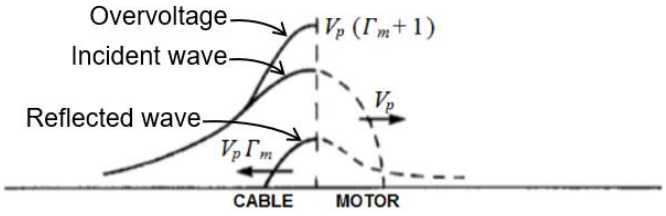


Fig. 1. Wave reflection at an impedance discontinuity at the boundary between the feeding cable and motor terminals, assuming that the motor impedance is higher than the cable impedance - adapted from [10].

$$V_m = V_p + \Gamma_m V_p = V_p\left(1+\frac{Z_m - Z_c}{Z_m + Z_c}\right) \tag{2}$$

Where Z_m is the motor impedance, Z_c is the cable impedance and V_p is the VSI pulse voltage amplitude.

Commonly the motor impedance Z_m is much higher than the cable impedance Z_c. Therefore, the reflection coefficient Γ_m is approximately *1*, and the motor terminal overvoltage V_m reaches nearly the double of the pulse voltage amplitude V_p.

Looking at the interface between VSI and cable, the VSI impedance Z_{vsi} is much lower than the cable impedance Z_c. Therefore, the reflection coefficient at VSI interface - Γ_{vsi} - is nearly *-1*. It means that the incident pulse $V_p\Gamma_m$ - reflected at the motor terminals - will be reflected at the VSI boundary with negative amplitude

$$\Gamma_{vsi} = \frac{Z_c - Z_{vsi}}{Z_c + Z_{vsi}}. \tag{3}$$

Therefore, another reflected pulse with $V_p\Gamma_m\Gamma_{vsi}$ amplitude will be directed to the motor terminals through the cable. Hence, a sequence of traveling waves will be moving forward and backward through the cable - consequence of reflections - superposing themselves, as shown in Fig. 2. Resulting in a transient motor terminal overvoltage represented in the Fig. 3.

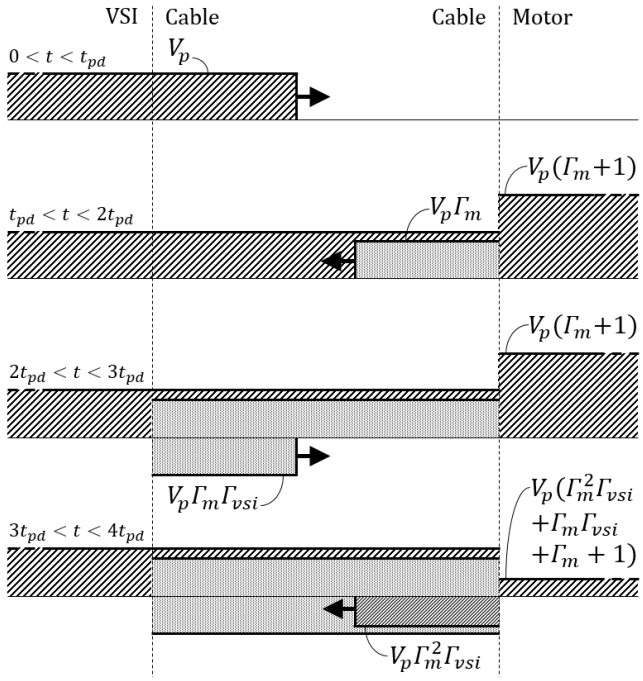
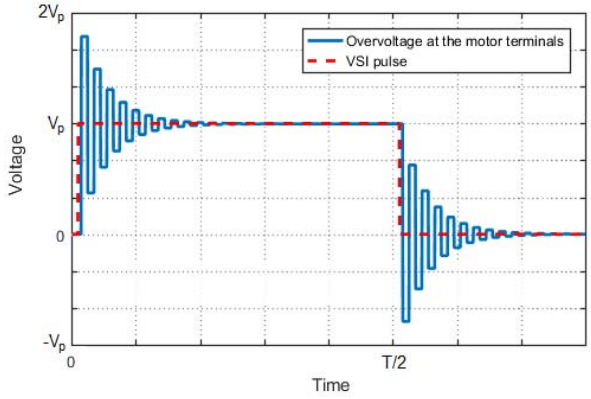
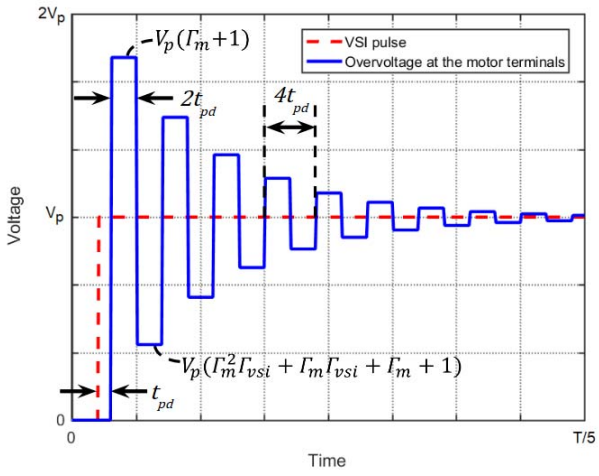


Fig. 2. VSI pulse reflections at both cables interfaces - cable/motor and cable/VSI - and motor terminal voltage oscillation.



(a)



(b)

Fig. 3. Transient motor terminal overvoltage due pulse reflections. (a) One pulse behavior. (b) Detail of overvoltage when pulse is rising.

After a pulse V_p arrives at the terminals the first time, the voltage amplitude at the terminals will change at any $2t_{pd}$ time interval. Considering that the first pulse will arrive at the terminals at $t=2t_{pd}$, at any instant multiple of $2t_{pd} - 2nt_{pd}$, with n as positive integer - the terminal voltage will change according to the previous voltage amplitude, incident pulse amplitude and its reflection pulse amplitude. In that condition, transient terminal overvoltage could be described as

$$V_{m_n} = \sum_{k=1}^{n} V_p\left(\Gamma_m^k\Gamma_{vsi}^{k-1} + \Gamma_m^{k-1}\Gamma_{vsi}^{k-1}\right). \tag{4}$$

In (4) the component that represents the incident pulse amplitude is $V_p\Gamma_m^{n-1}\Gamma_{vsi}^{n-1}$ and the component $V_p\Gamma_m^n\Gamma_{vsi}^{n-1}$ represents the reflected pulse amplitude and the sum of components from *1* to *n-1* represents the previous state of motor terminal voltage. For a single step pulse, voltage peak will occur for *n=1*.

III. Active Overvoltage Mitigation

The simple idea of using parallel VSI or three-level VSI to feed a motor would not mitigate overvoltage, in fact it can enhance it, as seen in Fig. 4. If *n* identical parallel VSI with identical cables send pulses simultaneously to the motor, the cables will be in parallel, reducing the equivalent impedance.

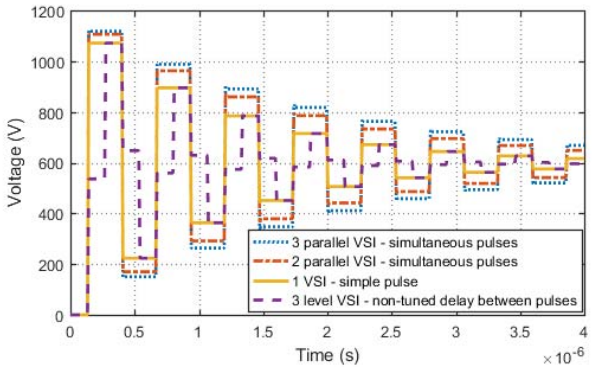


Fig. 4. Transient motor terminal overvoltage comparison for motor driven by one VSI with simple pulse, two and three parallel VSI sending pulses simultaneously and one three-level VSI with non-tuned pulses delay.

Lower equivalent cable impedance results in higher reflection coefficient, hence, higher overvoltage.

$$\Gamma_{m_n} = \frac{Z_m - Z_c/n}{Z_m + Z_c/n} = \frac{nZ_m - Z_c}{nZ_m + Z_c} > \Gamma_m \qquad (5)$$

$$\Gamma_{vsi_n} = \frac{Z_c/n - Z_{vsi}/n}{Z_c/n + Z_{vsi}/n} = \frac{Z_c - Z_{vsi}}{Z_c + Z_{si}} = \Gamma_{vsi} \qquad (6)$$

To achieve significant overvoltage mitigation using parallel VSI it is necessary to adopt a combined switching strategy to damp the amplitude of the traveling waves superposition at the motor terminals, as proposed by [9], [11], [12].

Reference [11] proposes a low loss active method for overvoltage mitigation with simple topology and considerable overvoltage reduction on the motor terminals due to combined switching strategy of parallel VSI. The motor will be driven by parallel VSI that will be both connected in a common point at the motor terminals by identical cables - same length and same impedance. The switching strategy will minimize the effects of the travelling reflected voltage pulses, by delaying pulses by two times the propagation pulse delay at the cable length ($2t_{pd}$). The superposition of the pulses will attenuate overvoltage. Topology and switching strategies are shown in Fig. 5.

Differently, [9] proposes a similar superposition of pulses delayed, however, just one three-level VSI is used (0, $+V_{dc}/2$ and $+V_{dc}$). The $+V_{dc}/2$ pulse and the $+V_{dc}$ pulse are delayed by two times pulse delay propagation at the cable ($2t_{pd}$), resulting in two identical pulses superposition at the motor terminals, as shown in Fig. 6. Moreover, as proposed in [12], if the intermediary voltage of the three-level VSI is adjustable, it is possible to mitigate terminal motor overvoltage to negligible levels. It occurs when intermediary DC voltage link V_{interm} is

$$V_{interm} = \left| \frac{2}{(\Gamma_m + 1)(\Gamma_{vsi} - 1)} \frac{V_p Z_m}{Z_m + Z_{vsi}} \right|. \qquad (7)$$

Where the term $V_pZ_m/(Z_m+Z_{vsi})$ represents the steady state voltage at the motor terminals and $2/[(\Gamma_m+1)(\Gamma_{vsi}-1)]$ represents the partition of the pulse that reflected at the motor terminals will reach the steady state voltage.

As long as the internal parameters of the topologies presented do not suffer any considerable variation, overvoltage mitigation will be effective. However, as soon as those parameters changes by thermal effects or any external condition, the overvoltage mitigation level degrades.

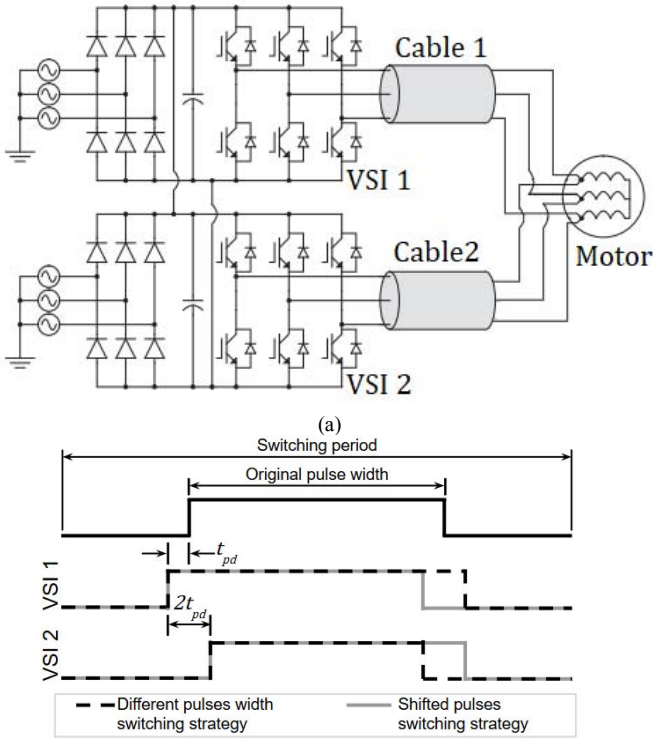


Fig. 5. Overvoltage mitigation method proposed by [11] with motor driven by two parallel VSI connected at a common point at the motor terminals by two parallel identical cables, with combined switching strategy. (a) Topology. (b) Switching strategy with first pulse $2t_{pd}$ wider than the original pulse and second pulse $2t_{pd}$ narrower than the original pulse, both centered - proposed by [11]. (c) Switching strategy proposed in this paper, two pulses identical to the original pulse, shifted by $2t_{pd}$.

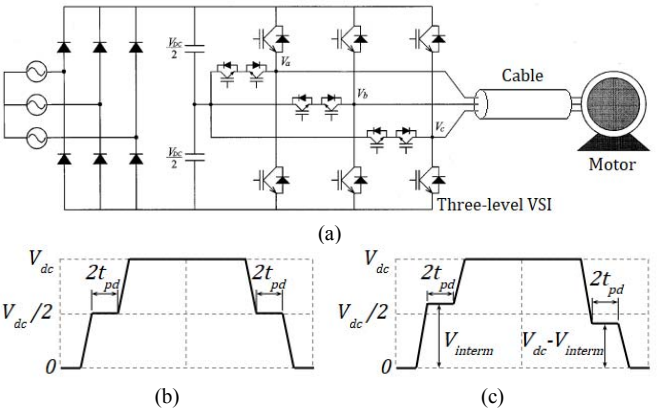


Fig. 6. Overvoltage method proposed by [9][12] with one three-level VSI with switching strategy. (a) Topology. (b) Switching strategy with intermediary voltage of $V_{dc}/2$ [9]. (c) Switching strategy with adjustable intermediary voltage [12].

IV. Methodology

To test the parameters vulnerability, we will use the simplest topology adopted by [11]: two parallel VSI, connected to a common point at the motor terminals by two identical cables. Both VSIs and cables have completely identical parameters. Topologies proposed by [9] and [12] will

also be compared and have some parameters analyzed.

As impedance of the cables may vary according to the power dissipation by Joule losses, currents behavior needs to be observed. In that sense, two different switching strategies will be tested in [11] topology.

The first one, proposed by [11], presents pulses with different widths. Compared with the first VSI pulse, the second VSI pulse rises delayed by two times the propagation pulse delay towards the cable length - $2t_{pd}$ - and falls in advance of two times the propagation pulse delay towards the cable length, as shown in Fig. 5. (b).

The second switching strategy presents pulses with identical width, but the pulse of the second VSI is delayed from the pulse of the first VSI by two times the propagation pulse delay towards the electric cable length, as shown in Fig. 5. (c).

In both cases proposed, as different pulses travels in the cables it is expected to have different currents circulating in each cable, also energy dissipation by Joule effect should be different, causing a non-simultaneous cable heating and impedance variation.

The condition of cable impedance mismatch and its impacts on overvoltage mitigation will be simulated and the results will be discussed.

V. Results

The proposed topology was tested by simulation in PSpice®.

The simulation parameters adopted and shown in Table I are identical to the parameters used by [11] in simulation.

As a first step, we compare the overvoltage using two parallel VSI with combined switching strategy and using one three-level VSI as presented in methodology for benchmarking. Curves are shown in Fig. 7.

The overvoltage at the motor terminals when using one VSI with simple pulse - as shown in Fig. 4 - is 1 071.0 V (178.5% overvoltage). Using two VSI with both switching strategies proposed, the resulting overvoltage was reduced to 637.9 V (106.3% overvoltage). When using one three-level VSI with non-adjustable intermediary voltage, overvoltage was reduced to 647.3 V (107.9% overvoltage). Adopting three-level VSI with adjustable intermediary voltage, overvoltage is completely mitigated, except for the switching spikes that reach 603.7 V (100.6% overvoltage).

For the two parallel VSI configuration, the currents circulating over the cables are different, as shown in Fig, 8. Also, different switching strategies implies in different current circulation behavior.

Current in cable 1 is higher than in cable 2. The heat dissipation as Joule effect is proportional to the square of the current [13]. With different width pulses switching strategy, in the first pulse cycle, cable 1 dissipates 28.5% more energy than cable 2 by Joule effect. With shifted pulses switching strategy, cable 1 dissipates 28.8% more energy than cable 2 by Joule effect in the first pulse cycle.

As cables have different current circulation and power dissipation, and supposing similar cable heat dissipation rate to the ambient, it is expected that cables conductor heating rate to be different. Then, cable 1 would heat faster than cable 2, hence, resistivity at cable 1 conductors should rise faster than in cable 2. That non-homogeneous cables impedance variation will generate cables impedance mismatch.

Fig. 9 shows a comparison of overvoltage and current

TABLE I
Simulation Parameters

V_p [V]	Z_{vsi} [Ω]	Z_c [Ω]	Z_m [Ω]	t_{pd} [ns]	Γ_m	Γ_{vsi}	V_{interm} [V]
600	5	100	1 500	133	0.875	-0.905	334.884

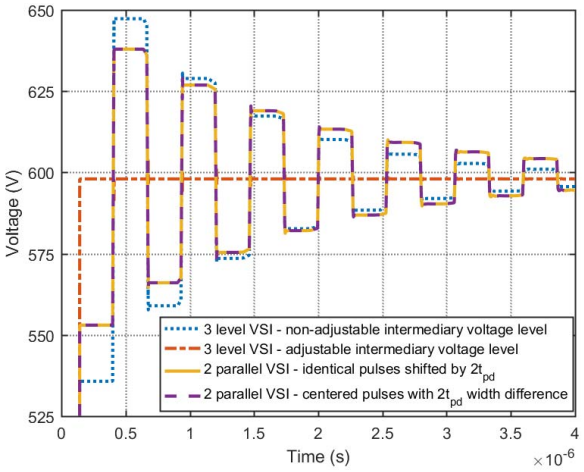


Fig. 7. Overvoltage comparison between motor driven by two VSI with combined switching strategy and motor driven by one three-level VSI with switching strategy delaying the two levels of the pulse.

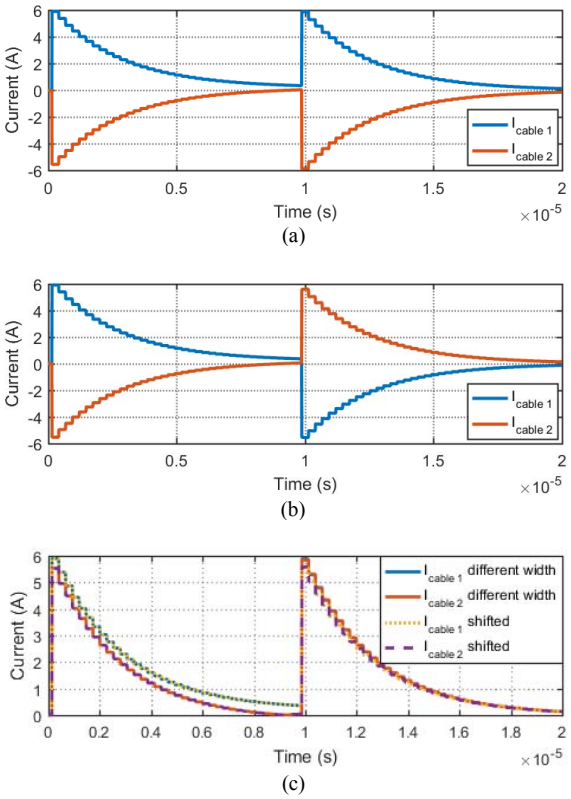


Fig. 8. Currents circulating in cable 1 and cable 2. (a) Different width pulses switching strategy. (b) Shifted pulses switching strategy. (c) Absolute current amplitudes comparison.

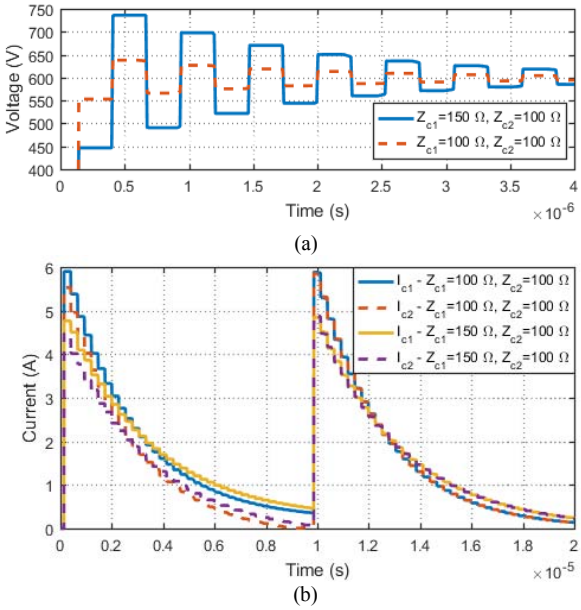


Fig. 9. (a) Overvoltage and (b) current for matched and mismatched cables impedances.

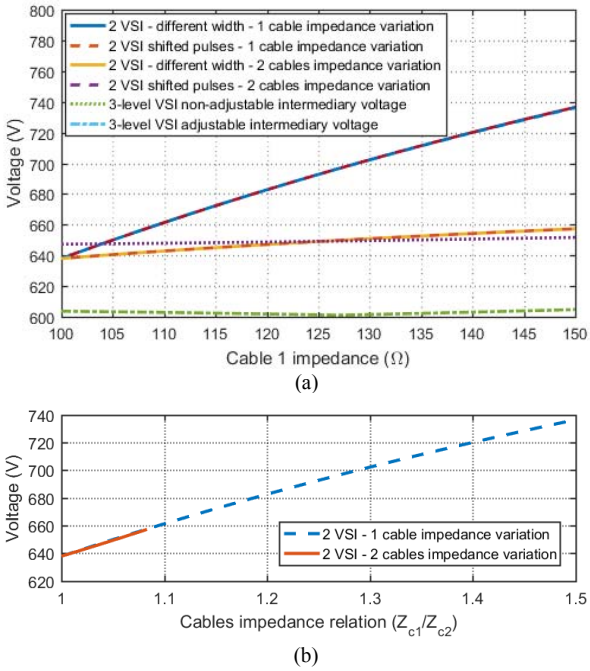


Fig. 10. Overvoltage comparison between motor fed by two parallel VSI with cables with same impedance and fed by two parallel VSI with cable mismatch impedance.

circulation for a matched cable impedances case (both cables with 100 Ω) and a mismatched cable impedances case (cable 1 impedance is 150 Ω and cable 2 impedance is 100 Ω).

As seen in Fig. 9, overvoltage mitigation degrades when cables impedances are mismatched. When cable 1 impedance becomes higher than cable 2 impedance, overvoltage becomes higher, currents amplitude at the cables becomes lower. However, currents circulation behavior remains the same, and power dissipation relation between cables still around 30%.

A precise transient cable heating calculation can be hard-working. Instead of a precise calculation of cable impedances mismatch, we will simulate two different scenarios to observe mismatched impedances impact in overvoltage: In the first scenario, the cable 1 impedance will vary and cable 2 impedance will remain constant. In the second scenario, impedances of both cables will vary, but cable 1 impedance variation rate will be 30% higher than cable 2 impedance variation rate, following the dynamic of power dissipation rate difference between cables 1 and 2.

Fig. 10 presents both scenarios. In the first scenario, overvoltage mitigation degrades in function of cable 1 impedance raising, 50.0% impedance raise represents 15,4% overvoltage raise. Results are identical for both switching strategies. For the second scenario, overvoltage also degrades in function of cable 1 and cable 2 impedance raising, but less than in scenario 1, 50.0% cable 1 impedance raise and 38.5% cable 2 impedance raise represents 3,0% overvoltage raise.

In fact, overvoltage is impacted by mismatched impedances - as shown in Fig. 10 (a). Different impedances of each cable imply in different reflection coefficients for each cable, hence, reflected pulses from each cable have different amplitude and cannot assure optimal overvoltage mitigation superposing themselves. Higher difference between cables impedances imply in higher overvoltage. Fig. 10 (b) compares the two scenarios by means of Z_{c1}/Z_{c2}. It shows that however the difference between Z_{c1} and Z_{c2} the relation Z_{c1}/Z_{c2} is almost linearly proportional to overvoltage raising.

As methods [9][12] uses just one cable, overvoltage variation in function of Z_c variation is low. It affects pulses amplitudes at the same rate, hence, overvoltage mitigation by pulse superposition is not compromised.

VI. Conclusion

Active overvoltage mitigation method by two parallel VSI and by three-level VSI has been discussed, compared and analyzed from the point of view of topology complexity, effectiveness and mismatched impedances vulnerability.

All methods discussed in this paper are effective. The three-level VSI with adjusted intermediary voltage proposed by [12] shows the better overvoltage response and low vulnerability to cable impedance variation, however, dynamical intermediary voltage adjustment and switching strategy may be complex to implement. The two parallel VSI methods proposed by [11] have simple topology - easy to implement - and mitigates overvoltage to low levels, on the other hand, the impedance mismatch vulnerability can degrade overvoltage mitigation.

It is important to emphasize that the mismatched impedance vulnerability seen will take place in heating cable transient. In steady state, cables will be in thermal equilibrium, and impedances will be matched. Furthermore, even with high cable impedances mismatch, overvoltage will be much lower than when the motor is driven by one VSI with simple pulses.

Further studies and assessments must be carried on to fully understand all parameter variations that could interfere on the overvoltage mitigation methods discussed in this paper. Moreover, some parameters such as signal transmission attenuation over cables may be taken into account for more precise results.

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