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Temperature and Bias Effects on Sputtered Ceria Diffusion Barriers for Solid Oxide Fuel Cells

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The effects of both temperature and applied bias power during the sputtering of gadolinia-doped ceria (GDC) interlayers used as diffusion barriers in anode-supported solid oxide fuel cells (SOFCs) were studied. Scanning electron microscopy analysis revealed that increasing the applied bias power, in the 0–300 W range, increasingly promotes the deposition of continuous and dense interlayers. Such feature was mirrored in the electrochemical performance of single cells that exhibited ~15% enhancement of the power density of an SOFC with bias-assisted sputtered interlayers. In addition, fuel cells having interlayers deposited in the 400–800°C temperature range exhibited similar microstructure and electrochemical performances, indicating that the applied bias allows for the sputtering of GDC protective interlayers at relatively lower temperatures than unbiased depositions. The presented results evidenced that bias-assisted sputtering is an effective technique for the fabrication of high performance anode-supported SOFCs.
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Diffusion barrier interlayers have been increasingly investigated as a convenient method to avoid undesired reactions between component materials in solid oxide fuel cells (SOFCs).[1-3] The need for such protective interlayers arises from the utilization of alternative materials that replace conventional components and aim at high performance SOFCs. However, such alternative materials usually present interdiffusion of chemical species along the electrolyte/electrode interfaces, which results in a rapid degradation of the fuel cell properties. Conventional SOFCs, using yttria-stabilized zirconia (YSZ) support electrolytes, Ni/YSZ cermets, and doped lanthanum manganites (for example lanthanum strontium manganite, LSMs), exhibit relatively good performance when operating at high temperatures (800–1000°C).[4] Nevertheless, such high operating temperatures are directly related to severe limitations in terms of material choice, thermal stability, and high cost of the device, those being relevant issues requiring further developments for bridging the gap to the commercialization of SOFCs.[4,5] Research efforts to overcome the imposed restrictions due to the high operating temperature have led to the development of intermediate-temperature SOFCs.[4]

One of the main contributions to reduce the operation temperature is the development of anode-supported SOFCs with a thin (~10 μm) YSZ electrolyte.[4-6] However, when the operation temperature is decreased to intermediate values, in the 500–800°C range, the kinetics of electrode processes is affected. Particularly, the overpotential loss due to the LSM-based cathode is the most significant one when the anode-supported SOFC operates at temperatures significantly lower than 800°C.[4,5] In this context, mixed ionic–electronic conductors have been proposed as substitutes for the LSM cathode. Among them, the lanthanum-doped cobaltite ferrite $(La,Sr)(Co,Fe)O_{3-\delta}$ (LSCF) has been considered as a promising cathode due to good electrical and catalytic properties that contribute to higher performance at intermediate temperatures.[7,8] Nonetheless, LSCF has appreciable reactivity with the YSZ electrolyte, and the interdiffusion of Sr^{2+} ions across the cathode/electrolyte interface is responsible for the formation of resistive phases that rapidly degrades the performance of the SOFC.[1,2,7,9]

To prevent the interdiffusion of species between the two superposed materials, ceria-based interlayers have been used as a diffusion barrier between YSZ and LSCF due to reasonable inertness and good electrical properties.[1,2,9] One of the main challenges regarding diffusion barriers is the fabrication of cost-effective and reproducible protective interlayers at sufficiently low temperatures to avoid undesired reactions. The effectiveness of the diffusion barrier is closely related to its microstructural properties, and dense and homogeneous interlayers are advantageous. Previous studies evidenced that single cells with ceria interlayers fabricated by reactive magnetron sputtering (RMS) exhibited significantly enhanced performance when compared to those fabricated by wet ceramic deposition techniques.[1,10] Such an improved performance is possibly associated with the higher homogeneity and density of sputtered layers, which do not require an additional sintering step at temperatures that can promote a reaction between doped ceria and YSZ.[1,10]

Although sputtering is known as a stable, reproducible, and scalable industrial process, further investigation is required for the fabrication of optimized SOFC protective interlayers. Several RMS parameters, such as substrate temperature, gas pressure, and applied bias voltage, can be controlled for optimized depositions. The growth of sputtered films is influenced by both the sputtering rate, determined by the energy and flux of incident particles, and the sputtering temperature (the temperature of the substrate). The sputtering temperature is a critical parameter that influences the grain size and also the density and type of microstructural defects of the deposited film. Higher sputtering temperature leads to an enhanced mobility of depositing atoms on the substrate plane and long-range diffusion processes start to play an important role in the growth of the film. During the sputtering process, the growing film is bombarded by many particles, both charged and neutral. Although it is difficult to control the neutral particles, a negative applied bias modifies the potential distribution along the sputtering chamber, accelerating positively charged ions onto the substrate and transforming the substrate to a secondary sputtering target. The overall effect of the applied bias voltage is the change in both the energy and flux of particles bombarding the substrate, and because the nucleation and growth processes are closely related to this bombardment, essentially, every property of the sputtered films can be controlled by the bias voltage applied during deposition. In fact, bias-assisted sputtering produces films with enhanced microstructural and electrical properties when compared to those of unbiased depositions.[6,11,12]

In the present study, the effects of both temperature and applied bias voltage during sputtering of gadolinia-doped ceria (GDC) diffusion barriers over YSZ electrolytes were studied. The experimental findings indicate that bias-assisted sputtering has a marked effect on the microstructure of the interlayers and allows the fabrication of dense GDC barriers at relatively low temperatures, a feature that was reflected on the performance of a single anode-supported SOFC.

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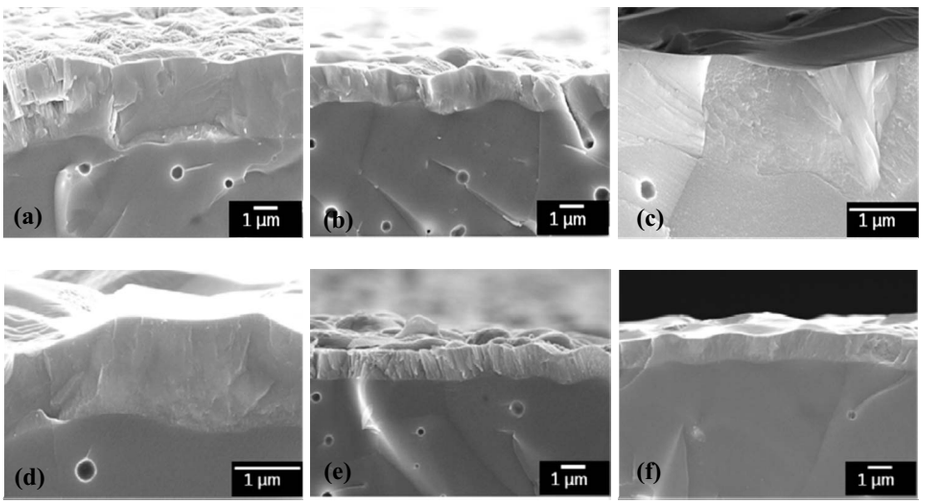

Figure 1. Cross-sectional micrographs of GDC interlayers sputtered at 800°C with applied power bias (a) 10, (b) 100, (c) 300 (with 16 sccm O_2 flow), and (d) 300 W (with 8 sccm O_2 flow); samples sputtered at 400°C with applied power bias (e) 50 and (f) 300 W (with 16 sccm O_2 flow).

Experimental

Half-cells comprising a Ni/YSZ anode support and an anode functional layer and a YSZ electrolyte were used as substrates for the deposition of $Ce_{0.8}Gd_{0.2}O_{2-\delta}$ interlayers. The half-cell substrates were fabricated following the procedures developed at Forschungszentrum Jülich and further details regarding cell fabrication are described elsewhere.[13] Coatings were carried out in a physical vapor deposition system CS 400ES (Von Ardenne Anlagentechnik). The surface of the substrates was first cleaned with organic solvents and conditioned by sputter-etching (0.6–0.9 W cm^{-2} for 10 min). Then, specimens were transferred to the sputtering chamber without breaking the vacuum and heated to the deposition temperature (400, 600, or 800°C) with a 3 K min^{-1} rate. A metallic target, with a nominal composition of 80 atom % Ce and 20 atom % Gd (99.7% purity), under 16 sccm oxygen flow was used to grow GDC interlayers by reactive magnetron dc sputtering. Different oxygen flow rates (8, 16, and 32 sccm) were used to evaluate the influence of oxygen flow on the deposited layer, and the flow rates of the samples fabricated under such conditions are indicated in the text. The base pressure in the process chamber was 10^{-6} Pa. The dc sputtering energy was set to 500 W and a high frequency bias voltage with a frequency of 13.56 MHz was applied to the metallic sample holder by controlling a fixed bias power, ranging from 0 to 300 W. The growth rate dependence on the applied bias was studied by fixing the total energy of the deposition process to 2 kWh. By assuming a linear growth rate, GDC layers with ~1 μm thickness were fabricated by adjusting the deposition time for each applied bias (0, 50, 100, and 300 W) at different temperatures. Previous energy-dispersive X-ray spectroscopy and X-ray diffraction data confirmed the fluorite structure of sputtered GDC interlayers.[1] Field-emission gun electron scanning microscope (FEG-SEM, Zeiss Ultra 55) analyses were performed in both fractured cross sections and surfaces of the deposited interlayers. The thickness of the interlayers was estimated by taking several FEG-SEM images in different areas of the samples, and the average thickness values were calculated by considering about 15 measurements.

Single cells were fabricated by screen printing a $La_{0.58}Sr_{0.4}Fe_{0.8}Co_{0.2}O_{3-\delta}$ (LSFC) cathode onto the GDC interlayer. Details concerning the preparation of both LSFC powder and suspension are reported elsewhere.[1] Cathode sintering was carried out at 1040°C for 3 h in air. The final thickness of the cathode layer was ~60 μm and the active area of the single cells was ~40 × 40 mm.

Electrochemical tests were performed in the 600–850°C temperature range under hydrogen (3 vol % H_2O) and air, both set at 1000 mL min^{-1} flow rate. Electrical contacts were made by Ni and Pt meshes used at the anode and cathode sides, respectively. Polarization curves were collected by dc measurements using a current-control power supply and a computer-controlled data acquisition system. The recording of current–voltage (*I-V*) curves is conducted

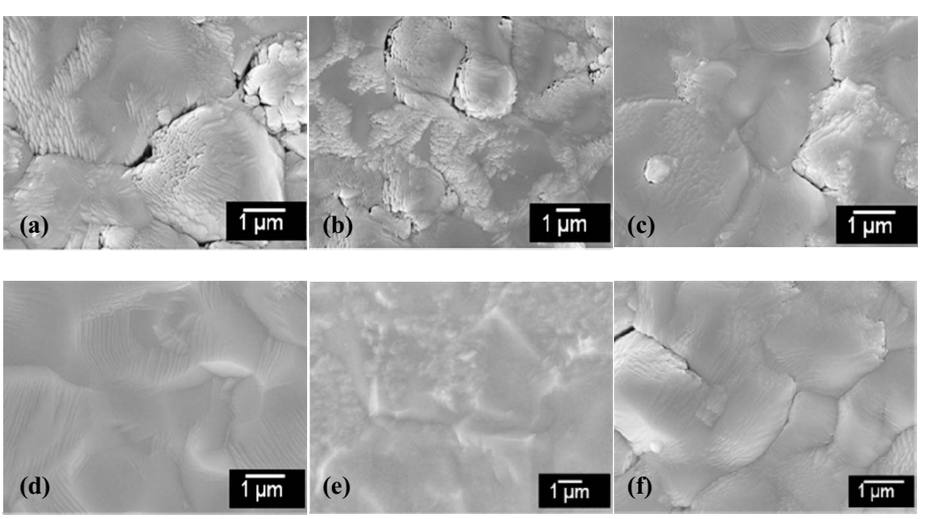

Figure 2. Surface micrographs of the of GDC interlayers sputtered at 800°C with applied power bias (a) 10, (b) 50, (c) 100, and (d) 300 W; samples sputtered at 400°C with applied power bias (e) 100 and (f) 300 W.

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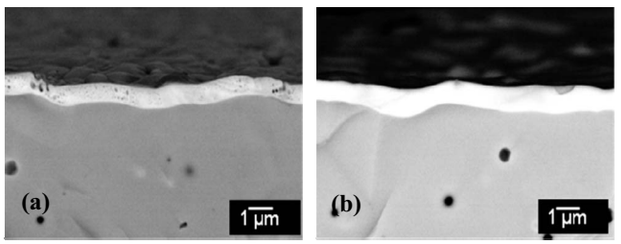

Figure 3. Backscattered electrons micrographs of the cross section of GDC interlayers sputtered at 800°C with applied power bias (a) 50 and (b) 300 W sintered at 1080°C. The GDC interlayer is identified as the brighter regions.

under galvanostatic control starting at the open-circuit voltage (OCV) using a current step size of 0.0625 A/cm^2. For all studied samples, sputtered at different temperatures and/or applied bias voltages, a set of three nominally identical unit cells was produced and measured.

Results and Discussion

Detailed FEG-SEM analyses were performed to investigate the effect of applied bias power on the microstructure of deposited GDC interlayers. Figure 1 shows secondary electron FEG-SEM micrographs of fractured cross sections of half-cells in the region of the interface between the YSZ electrolyte and the GDC interlayers sputtered at 400 and 800°C with different applied power biases. The GDC protective barrier is clearly identified as a continuous and homogeneous layer, with thickness in the 1–2 μm range, deposited over the YSZ electrolyte. The experimental results indicated that for reactive magnetron dc sputtering depositions carried out at 800°C, increasing the applied bias power decreased markedly the growth rate from ~19 nm min^{-1} in the 0–10 W applied bias range to ~10 nm min^{-1} in the 100–300 W range.[6,11] At the deposition temperature of 400°C, the growth rate was less dependent on the applied bias power, and samples deposited at 300 W have growth rates ~8 nm min^{-1}. The lower growth rate observed at high applied bias values can be associated with the resputtering of feebly deposited GDC because samples become a secondary sputtering target when bias power is applied to the substrate.[12] However, it is more likely that the lower thickness of the biased GDC interlayers is related to the increased density of the sputtered layers.

The growth rate and microstructure of samples deposited at 800°C and 300 W were also investigated as a function of the O_2 flow during the RMS process. The micrographs shown in Fig. 1c and d for samples sputtered with 8 and 16 sccm O_2 flow, respectively, indicate that oxygen stoichiometry has no significant influence on the evolution of the microstructure of the sputtered interlayers. Samples sputtered at different O_2 flow rates in the range of 8–32 sccm have similar microstructures and growth rates within the experimental accuracy.

Figure 2 shows FEG-SEM images of the surfaces of GDC interlayers deposited with different experimental conditions. Agreeing with the cross-sectional images (Fig. 1), a remarkable effect of the applied bias on the surface microstructure of GDC interlayers can be observed in Fig. 2: Biased RMS depositions resulted in interlayers with more continuous and homogeneous microstructures. The main feature revealed by the FEG-SEM results displayed in both Fig. 1 and 2 was the increase in the density of GDC interlayers with increasing applied bias power. With regard to the deposition temperature and the melting point of GDC, sputtered GDC films usually exhibit a characteristic columnar structure resulting from the growth mechanism. Such an inhomogeneous microstructure is associated with remnant islands, formed in the initial growth stage, which did not attain the coalescence stage completely and limited the continuity of the sputtered layer.[12] This columnar structure is clearly observed in some regions of unbiased depositions and samples sputtered with applied bias power below 100 W (Fig. 1a and e and 2a, b and e).[1,10] However, increasing the applied bias power progressively inhibited the columnar structure of sputtered interlayers and favored a more homogeneous, continuous, and dense microstructure. Such a feature was observed for different temperatures of depositions and is more evident for samples sputtered at high applied bias (≥50 W). The effect of substrate bias on film microstructure has been explained in terms of ion bombardment and redeposition of film ma-

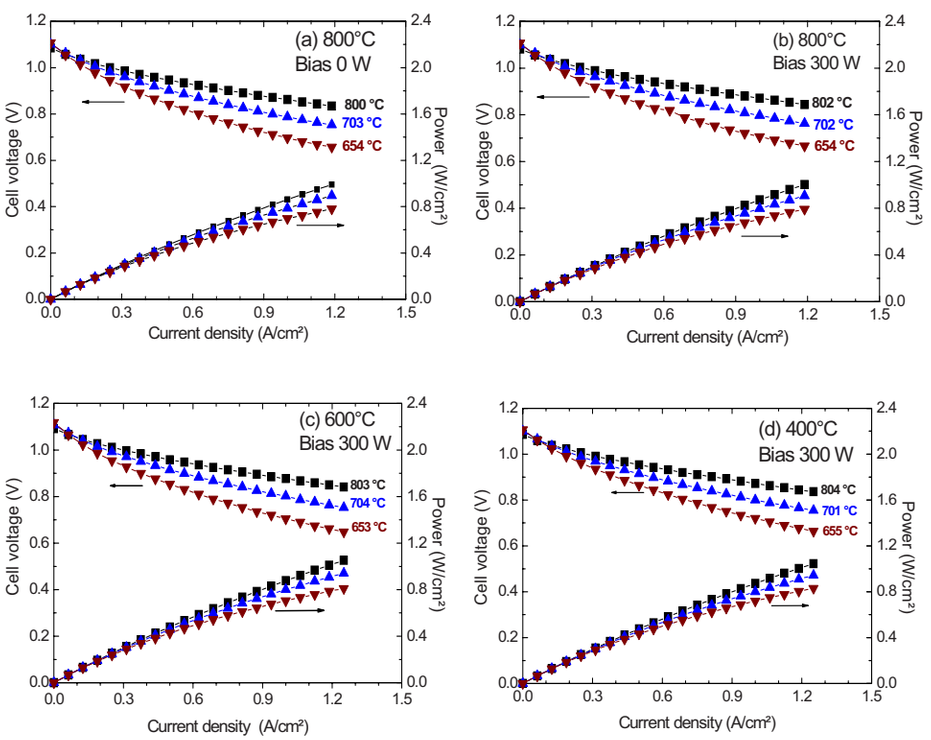

Figure 4. (Color online) Polarization (left *y*-axis) and power density (right *y*-axis) curves measured in the 650–800°C range for single cells with GDC interlayers sputtered at different temperatures and applied bias powers: (a) 800°C – 0 W, (b) 800°C – 300 W, (c) 600°C – 300 W, and (d) 400°C – 300 W.

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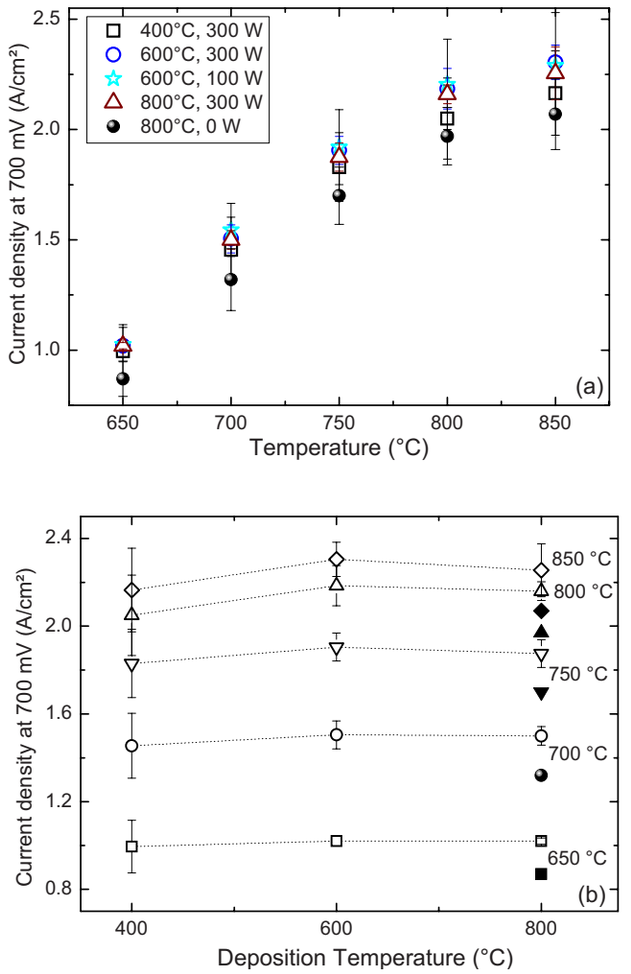

Figure 5. (Color online) Current density at 700 mV of single cells with sputtered GDC interlayers as a function of (a) measuring temperature and (b) sputtering temperature of samples deposited with 300 W applied bias power at different measuring temperatures. Solid dots indicate the unbiased deposition and error bars correspond to the averaged values of nominally identical samples.

terial. Such combined effects promote the removal of material from protrusions, redeposition into pores, and eventual film surface planarization.[6] Even though compressive stress could play a role in bias-assisted sputtering, the deposited interlayers exhibit good quality, and neither delamination nor cracking was observed.[14]

The fabrication of SOFC single cells involves both the deposition and sintering of the cathode after the sputtering of the diffusion barrier. Thus, the effect of cathode sintering was simulated by heat-treatment at 1080°C for 3 h in air to study its influence to the microstructure of deposited GDC interlayers, especially concerning the formation of cracks due to a possible lateral shrinkage of the CGO layer. Figure 3 shows backscattered electron images of the cross section of the samples sputtered at 800°C with an applied power bias of 50 and 300 W after heat-treatment at 1080°C. The observed microstructures suggested that the heat-treatment for cathode sintering smoothened the columnar structure but was not effective to promote the densification of the GDC interlayer. Samples deposited with low applied bias power ($\leq$50 W) retain residual porous regions that are probably related to the former columnar regions, whereas the 300 W biased sample maintains a dense microstructure.

By assuming a linear growth rate, GDC layers with $\sim$1 μm thickness were sputtered onto half-cells by adjusting the deposition time for each applied bias power (0, 50, 100, and 300 W). After cathode deposition and sintering, single cells with sputtered GDC interlayers were assembled for electrochemical tests. Figure 4 shows typical polarization (*I-V*) curves, measured in the 650–800°C range, of a single SOFC with sputtered GDC interlayers with 300 W applied bias power at different temperatures and the unbiased deposition carried out at 800°C. The polarization curves exhibited characteristic features of state-of-the-art anode-supported SOFC single cells with power densities exceeding 1 W cm^{-2} at 800°C and $\sim$800 mV. At first inspection, the electrochemical properties of the fuel cells showed no significant dependence on both the applied bias power and deposition temperature: measured OCVs were $\sim$1.1 V and the ohmic drop polarization was the most significant one in the investigated current range.

A more detailed analysis evidenced an increase in the performance of fuel cells having biased RMS deposited interlayers. To better analyze the effect of sputtering temperature and applied bias power on the performance of fuel cells, averaged values of current density extrapolated at 700 mV were calculated from polarization curves measured for at least two nominally identical samples. Figure 5a and b displays the current density at 700 mV as a function of both the *I-V* curve measuring temperature and the sputtering temperature, respectively.

The results shown in Fig. 5 demonstrated that single cells with GDC interlayers sputtered with $>$100 W bias displayed up to $\sim$15% increased current density values when compared to the unbiased deposition at 800°C in the entire temperature range measured. Nonetheless, a direct correlation between either the applied bias power or the sputtering temperature and the obtained current density values was not clear. Such a behavior may be attributed to small differences of the interlayer thickness or in the morphology of the interlayer, which can be present even in nominally identical cells. This point requires further experiments to be better evaluated. Figure 5 evidences that fuel cells with GDC interlayers sputtered with high applied bias at relatively low temperatures (400–600°C) have similar microstructure and comparable electrochemical performance to the ones sputtered at 800°C. Increasing the sputtering temperature favors the fabrication of more homogeneous interlayers due to a higher mobility of deposited atoms. Previous studies of the unbiased RMS of GDC interlayers showed that depositions carried out at 800°C resulted in interlayers with better properties than depositions at lower temperatures, a feature related to both the higher density of the interlayer and good adhesion between the electrolyte/interlayer/cathode interfaces.[1,10] The present results indicate that ion bombardment and redeposition of film material taking place in bias-assisted sputtering contributes to enhanced microstructural properties of GDC interlayers. Such a feature allows for the deposition of homogeneous and dense barrier layers at relatively lower temperatures, which avoid undesired reactions between the components and are likely to result in better properties of the fuel cell.

Conclusion

The influence of both the deposition temperature and the applied bias power on the properties of magnetron sputtered GDC diffusion barriers was studied. The applied bias has a marked effect on the microstructure of ceria-based interlayers that was reflected on the electrochemical performance of anode-supported SOFCs. Ceria-based interlayers sputtered, in the 400–800°C range, with 300 W applied bias power have similar electrochemical performance independent of the deposition temperature. The experimental data indicated that the applied bias is a useful tool that improves the quality of diffusion barriers and allows for the sputtering of high performance ceria-based interlayers at lower temperatures than unbiased depositions.

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